International Journal of Electronics and Communication Engineering (IJECE)
ISSN(P): 2278-9901; ISSN(E): 2278-991X
Vol. 5, Issue 3, Apr - May 2016; 41-50

International Academy of Science, Engineering and Technology
Connecting Researchers; Nurturing Innovations

QUANTUM DOT CELLULAR AUTOMATA BASED PARITY GENERATOR AND DETECTOR: A REVIEW

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ABSTRACT

Quantum dot cellular automata (QCA) is a computing approach, in which binary information is represented as the charge configuration among the quantum dots. In nanoscale integrated circuit energy consumption and area utilization are a major concern, hence in recent years QCA has attracted a lot of attention as a result of its extremely small feature size and low power consumption. This technology is best suited for the semiconductor fabrication because of its less time consuming and less expensive methods. As per Moore's law, number of transistors in an integrated circuit doubles for every two years, fabrication process faces some technical barriers. In context of this, QCA has emerged as the most promising technology, as an alternative to CMOS technology. In this paper efforts have been made to show the work carried out on QCA and focused on the science and technology applications of QCA due to its many interesting and important applications such as parity generator and checker.

KEYWORDS: Quantum Dot Cellular Automata, Nano-Electronics, QCA Clocking, Majority Gate, QCA Designer, Parity Generator and Checker

INTRODUCTION

In the QCA approach,cell is the key element of this paradigm, each cell consists of four number of quantum dots [1].Dots are constructed from aluminum using electron beam lithography technique, similar to conventional lithography except that patterns are traced out using an electron beam rather than using a mask and light. The style of working in this technology, started with a quantum dot followed by quantum cells consists of four dots, after that gates are designed using cells and then appropriate circuits are designed at last, as shown in Figure 1(a). A dot, in this case, is simply a region in which charge is localized. Figure 1(a) illustrates a schematic four-dot QCA cell [2]. In our QCA system Figure 1(c) the cell consists of four small "dots". D_1 to D_4[3]connected in a ring by AlOx tunnel junctions. Each dot is also capacitively coupled to a gate via capacitance C_G. To determine the cell polarization, electrostatic potential is measured on dots[3]. A quantum dot is a semiconductor nanostructure that confines the motion of conduction band electrons, valence band holes, or excitons (bound pairs of conduction band electrons and valence band holes) in all three spatial directions [4]. There are four quantum dots at each corner of cell in which two electrons are released, these two electrons will try to occupy the farthest possible site with respect to each other due to mutual electrostatic repulsion. Since diagonal is the largest distance in square, there exist two such possible conditions as shown in Figure 1(b). The stages of cell are known as polarization denoted by P. Polarization is defined [5] by the equation 1.

$$P = \frac{(\rho_2+\rho_4)-(\rho_1+\rho_3)}{\rho_1+\rho_2+\rho_3+\rho_4} \quad (1)$$

Where, $\rho_m$denotes the electronic charge at dot 'm'. Polarization P = -1 denotes the state '0' and P = +1 denotes the state '1' [6].When the bit is changed from 1 to 0, there is no discharging of the capacitor as in the case of conventional CMOS. Hence, inQCA, there is no dissipation of energy during transition[7].The confinement can be due to columbic interaction [8], the presence of an interface between different semiconductor materials (e.g. in core-shell nanocrystal systems), the presence of the semiconductor surface (e.g. semiconductor nanocrystal), or a combination of these. QCA functions are based on Columbic interaction instead of current used in CMOS, so there is no leakage current. Additionally, it has major advantages such as low power consumption, high speed and small space consumption[9]. In QCA, devices are composed of cells, each device is constructed by arranging cells near each other in an appropriate layout.

The International Technology Roadmap for Semiconductors (ITRS) has introduced some alternative technologies that can replace the CMOS based approach in the near future. Some of them are, Resonant Tunneling Diodes (RTD's), Single Electron Tunneling (SET), Quantum Cellular Automata (QCA), Tunneling Phase Logic (TPL), Carbon nanotubes and Silicon on Insulator (SOI)[10]. Among all of these technologies QCA has emerged as most promising technology that will replace the CMOS in near future. In QCA, quantum dots are used for digital computation [11], hence it provides outstanding energy efficiency [12], high density [13], and fast computing devices [14].

5-6 years from now QCA will play very important role when physical fabrication will be done because of its higher device density and operation at room temperature. In near future it will replace CMOS technology in Mobile devices, ALUs, and Processors. Power usage will be lessen hence battery life will increase. Since it is nanoscale technology, area usage on the chip will be less. Researchers are doing prominent work on this technology and its possibilities seem endless.

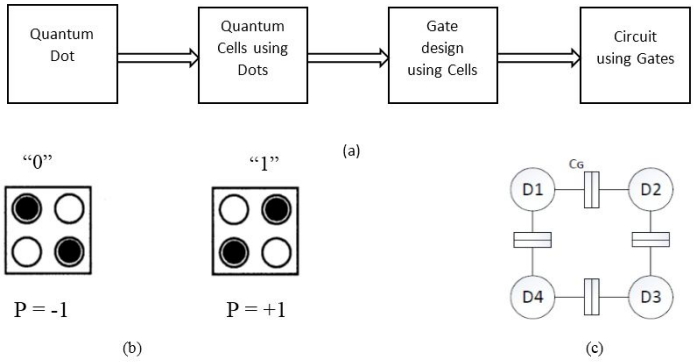

Figure 1: (A) Working Approach in QCA, (B)Two Possible States of 4 Dot QCA, (C) Schematic of our QCA System. The Cell is Defined by Dots D_1 to D_4connected in a Ring by Tunnel Junctions

For the very first, the idea of QCA was proposed in early 1940s by Von Neumann and Ulam [15]. Next in 1960s Conway introduced the Game of Life, which emulate QCA by modeling the interaction of cells based on mathematics [16] and multiple valued cellular automata dynamics and in 1990, Kikukazu Sakurai et al. introduced the organic QCA system models based on quantum dots. [17]. Later in the year 1993, Lent et al. experimentally enlightened the existence of QCA cell, with Aluminum Island acting as Quantum dots [18]. Unlike CMOS technology in which device and wire are made of different materials, QCA technology both wire and devices are made of QCA cell only.

STATE OF ART

Basic Logic Cells Design in QCA

Arranging cells in a row, as in Figure 2(a), results in a QCA wire, which transmits binary information as it is, from one end to the other[2]. Arranging two cells by touching the lower right corner of one cell to the upper left corner or upper right corner of one to lower left corner as in staircase form, it will act as the inverter as shown in Figure 2(b). If input is say A then output will be A'. There are two types of wire ordinary wire (90 degree) and rotated wire (45 degree) shown in Figure 2(c)[19].

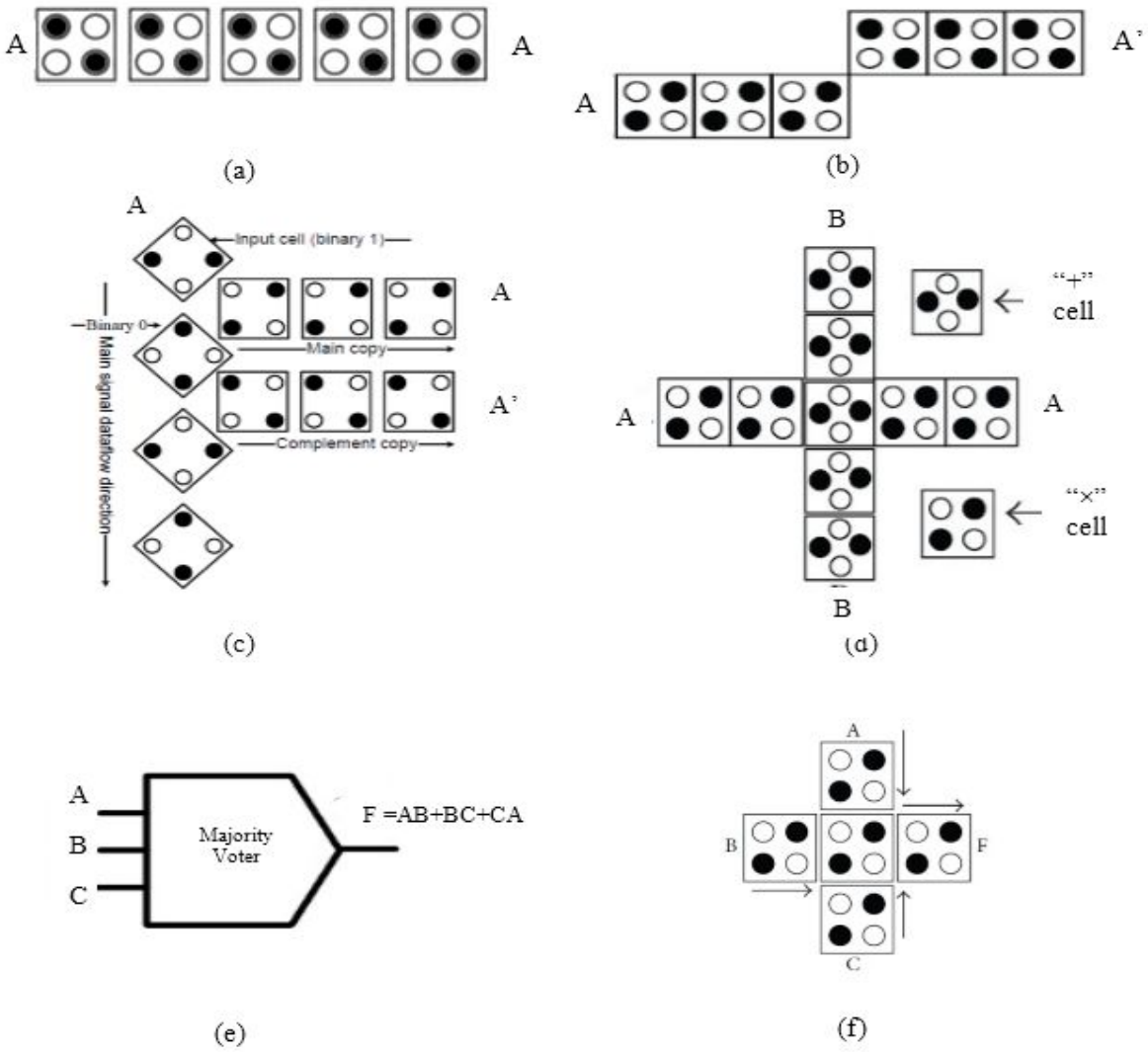

Figure 2: Basic Logic Cells in QCA: (a) QCA Wire, (b) Inverter, (c) Rotated Wire, (d) Wire Crossing, (e) Logic Representation of MV, (f) Cellular Laypot of MV

The main advantage of using 45 degree rotated wire is to overcome from crossovers for example if there are two signals say A and B, will cross each other without intervening to other signal if one signal(A) using 90 degree wire and another(B) using 45 degree as shown in Figure 2(d). Here 45 degree rotated cell is shown as "+" cell and 90 degree rotated wire is depicted as "×" cell[20]. Another logic gate which is also backbone for designing any logic circuit known as

Majority logic gate or Majority Voter (MV) gate. It consists of a cell surrounded by other four cells at each side of the square cell, Figure 2(e). This structure is also known as Von Neumann neighborhood structure[4]. Three of the side cells act as input (A,B & C) whereas the fourth cell (F) will give the output. The logic expression [21] of MV is defined by equation 2.

$$F(A,B,C) = AB + BC + AC \quad (2)$$

Using this equation we can derive the two universal gates used in digital electronics i.e. NAND &NOR gate. By setting the P = -1 to input C, it will act as an AND gate Figure 3(a) followed by an inverter will act as NAND gate. And by setting P = +1, MV will act as OR gate Figure 3(b).

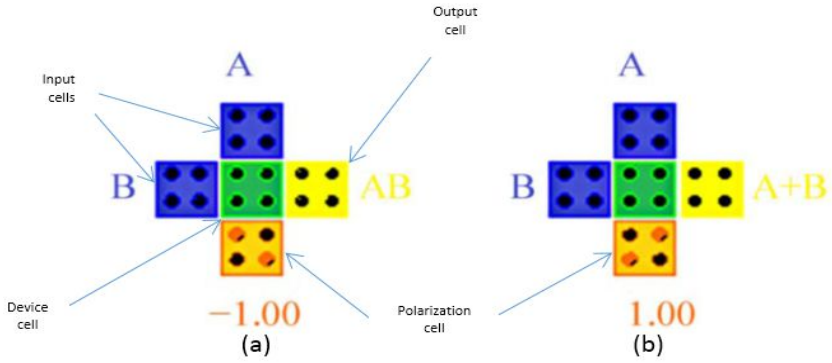

Figure 3: QCA Layout of A) AND Gate and B) OR Gate

$$F(A,B,0) = AB$$

$$F(A,B,1) = A + B$$

QCA Clock

Clock in QCA ismainly use for two purposes, first it controls the data flow and second to supply power to automation. Simply, clocking controls the information flow. The clocking of QCA can be realized by controlling the potential barriers between adjacent quantum-dots [22-24]. Unlike the CMOS circuit, which consists of an upper phase and a lower phase in its clock pulse, the clock pulse in the QCA technology has four operative aspects. No additional wire is needed for clocking the cells, since this property is naturally exists inside each of the cell[19].

The tunneling interruption are regularized with four separate stages as shown in Figure 4, the locking stage demonstrates that the tunneling barriers are raising, the locked stage point towards the fully raised situation of barriers. The relaxing stage shows that tunneling barriers are lowering and the relaxed stage determined that the tunneling barriers are absolutely lowered, allowing free electron movement within a cell [25]. When stages of clock 0 at locked stage and clock 1 at locking stage at same time then only data transfer take place from clock 0 to clock 1[26-34] and so on for the next clocks also, as shown in Figure 4.

Alternative names of these stages are also described by four different stages. During the **Switch** phase, the inter-dot barrier is slowly raised,and the QCA cell is established down to one of the two polarization states as forced by its neighbors. The inter-dot barrier is held high throughout the **Hold** phase, which resist the electron tunneling and therefore maintains the current ground polarization state of the QCA cell. The inter-dot barriers are lowered, and the excess electrons gain mobility till the **Release** and **Relax** phase respectively [35].

With the help of these four phases of clocking scheme, Information is advanced and forward sin QCA with in cells in settled timing scheme[36]. Thus every QCA circuit is divided into four areas and the series can be allocated to one of the four clock signals. With the help of this clocking system, the information is passed on to the various parts of the circuit through the cells one after another [37-38]. Figure 5 shows the four stages of a pulse.

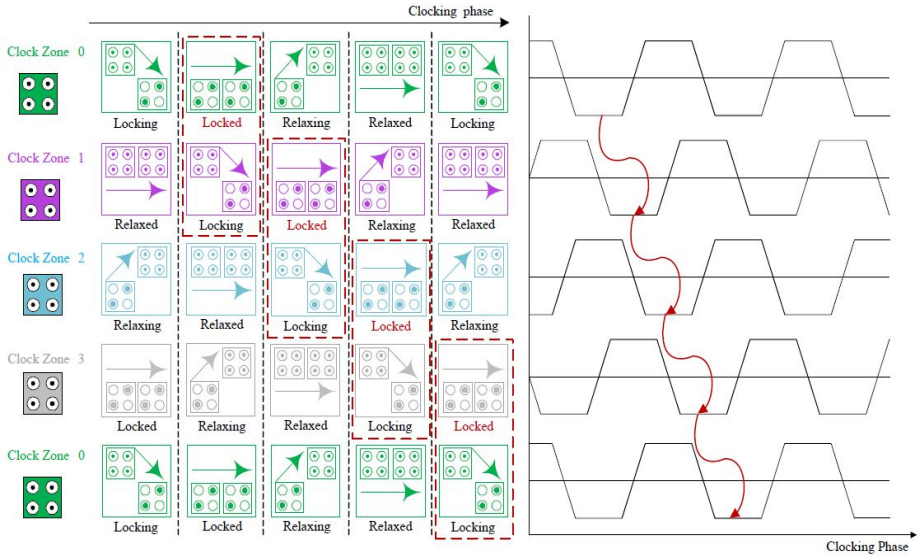

Figure 4: QCA Clocking Concept

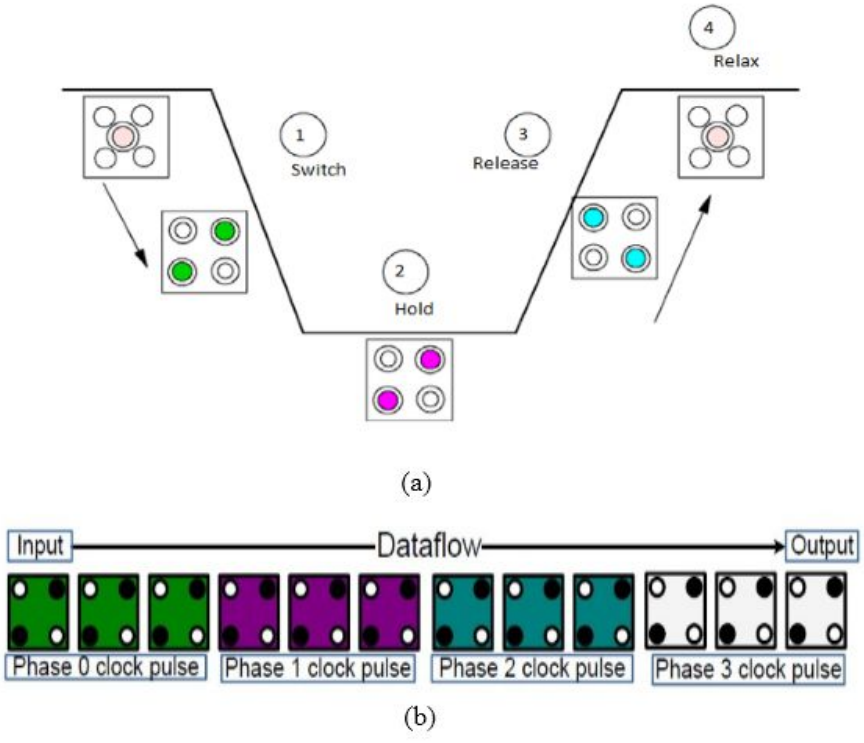

Figure 5: QCA Clock (A) Four Phases in a Clock Pulse, (B) Color Representing the Respective Clock Pulse

PARITY GENERATOR AND CHECKER METHODOLOGY

In recent years QCA is stimulated as a promisingarea in research of nanotechnology, to design nanoscalecircuits. In nanocommunication too, detection and correction of errors in a received message are major factors. On one side, device density, cost and power dissipation are the key factors in nanocommunication architecture. Parity is a concept to detect the errors.Hence variousparity generator and parity checker circuits in a nanocommunication architecture is studied. The detection of errors in the received message during transmission is also explored [39].

Parity Bit

The parity generating technique is one of the most widely used error detection techniques for data transmission. In digital systems, when binary data is transmitted and processed, data may be subjected to noise so that such noise can alter 0s to 1s and 1s to 0s. Hence parity bit is added to the word containing data in order to make number of 1s either even or odd. In this paper we shall be taking even parity everywhere. Thus it is used to detect errors, during the transmission of binary data. The message containing the data bits alongwith parity bit is transmitted from transmitter node to receiver node. At the receiving end number of 1s in the message is counted and if it doesn't match with the transmitted one, then it means there is an error in the data.

Parity Generator

Let us assume that a 3-bit message is to be transmitted with an even parity bit. Three inputs A,B, and C are applied to the circuits and output bit is the parity bit P. Truth table in Table 1, shows the even parity generator (PG) in which 1 is placed as parity bit in order to make al 1s as even when the number of 1s is in the truth table is odd.

$$P = A \oplus B \oplus C$$

Parity Detector

Even parity bit P generated at the transmitting end along with the three message signals is applied as the input to the parity checker (PC) circuit which checks the possibility of error on the data. Since data is transmitted with even parity, four bits received at circuit must have an even number of 1s. In case of error the received message consists of odd number of 1s. The output of the parity checker is denoted by parity error checker (PEC).PEC = 1 if the error occurs, i.e., the four bits received have odd number of 1s and PEC = 0 if no error occurs, i.e., if the four bit message has even number of 1s.

$$PEC = A \oplus B \oplus C \oplus P$$

Latency is the most important term to be focused on, in communication system. Latency explains the delay in the output. It must be minimum as possible. Message which is transmitted can be affected by noise in the medium, hence to get the exact message and to correct the errors at the receiver side, PG and PC circuits are used [5], [8], [25], [39], [43].

In the year 2003, Anjana et al [41], proposed the even and odd parity generator and checker, using 99and 145 no. of cells respectively, using the reversible logic gates, which occupied the 113724nm^{2}area on the silicon chip. In next year 2004, Shantanu et al [42], designed the PG and PC circuit which consume 52488nm^2 and 135432nm^2 respectively. Prominent researchers carried out their work with improvement of latency, which kept on decreasing periodically.Later on in the year 2015, Nandani rao et al [43], proposed the novel circuit on PG and PC with just only 47978nm^2 and 135024nm^2 respectively. We will carry out this work in continuation in the near future, it is expected to achieve the latency of only one

unit delay. Results of the various papers is also summarized in Table 1.

Table 1: Comparative Study of Parity Generator and Detector Circuits.

	No. Of Cells	Area (Nm^2)	%Age of Usage	Delay	
PG PC	99 145	113724 197316	28.20	3	Anjana et al.
PG PC	60 117	52488 135432	37.04	2	Shantanu et al.
PG PC	57 108	47978 135024	28.99	2	Nandani Rao et al.

QCA DESIGNER TOOL

QCA logic and circuit designers require a rapid and accurate simulation and design layout tool to determine the functionality of QCA circuits. QCADesigner gives the designer the ability to quickly layout a QCA design by providing an extensive set of CAD tools. As well, several simulation engines facilitate rapid and accurate simulation. It is the first publicly available design and simulation tool for QCA. Developed at the ATIPS Laboratory, at the University of Calgary, QCADesigner currently supports three different simulation engines, and many of the CADfeatures required for complex circuit design. [36], [44].

CONCLUSIONS

In this paper, a survey of various works is carried out in the field of QCA with respect to QCA cell, Majority gate, QCA clock, Parity generator, parity checker, as a first step towards the research on QCA. Only single bit or odd number of bitt error is detected by parity. There are many other possible applications of quantum dots in many different areas of science and technology like light emitting diode (LED), Photo voltaic cell and solar cells etc. The possibilities seems endless and future looks bright and exciting on all the possible applications of QCA. By this approach we can go for designing the logic gate with minimal area and latency for parity generator and detector.

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